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Docket No. AT9-99-287

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: **Cohen et al.** §

§ Group Art Unit: **2676**

Serial No.: **09/377,642** §

§ Examiner: **Tung, Kee M.**

Filed: **August 19, 1999** §

§

For: **Method and Apparatus for Performing Raster Operations in a Data Processing System** §

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

ATTENTION: Board of Patent Appeals and Interferences

Certificate of Mailing Under 37 C.F.R. § 1.8(a)
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By: Amelia C. Turner
Amelia C. Turner

APPELLANT'S BRIEF (37 C.F.R. 1.192)

This brief is in furtherance of the Notice of Appeal, filed in this case on October 14, 2003.

The fees required under § 1.17(c), and any required petition for extension of time for filing this brief and fees therefore, are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

This brief is transmitted in triplicate. (37 C.F.R. 1.192(a))

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REAL PARTIES IN INTEREST

The real party in interest in this appeal is the following party: IBM Corporation

RELATED APPEALS AND INTERFERENCES

With respect to other appeals or interferences that will directly affect, or be directly affected by, or have a bearing on the Board's decision in the pending appeal, there are no such appeals or interferences.

STATUS OF CLAIMS

A. TOTAL NUMBER OF CLAIMS IN APPLICATION

Claims in the application are: 1-6, 12-24, and 30

B. STATUS OF ALL THE CLAIMS IN APPLICATION

1. Claims canceled: 7-11, 25-29, 31, and 32
2. Claims withdrawn from consideration but not canceled: NONE
3. Claims pending: 1-6, 12-24, and 30
4. Claims allowed: NONE
5. Claims rejected: 1-6, 12-24, and 30

C. CLAIMS ON APPEAL

The claims on appeal are: 1-6, 12-24, and 30

STATUS OF AMENDMENTS

An after final amendment is filed herewith. The amendment cancels claims 11, 25-29, and 31 to place the application in better form for appeal by materially reducing or simplifying the issues for appeal. Since the amendments do not raise new issues that would require further search or consideration, Applicant respectfully requests that the amendments be entered upon filing an appeal.

SUMMARY OF INVENTION

The present invention provides a method and apparatus in a data processing system for performing a raster operation of graphics data. Specification, page 3, lines 3-5. A system memory and a video memory are included in the data processing system. Specification, page 3, lines 5-6. The system memory and the video memory are connected by a bus wherein the graphics data is organized into picture elements. Specification, page 3, lines 7-9. A plurality of picture elements is read from the system memory. Specification, page 3, lines 9-10. A plurality of picture elements is read from the video memory. Specification, page 3, lines 10-11. A raster operation is performed on the plurality of picture elements to form a plurality of processed picture elements. Specification, page 3, lines 11-13. The plurality of processed picture elements is written to the video memory. Specification, page 3, lines 13-15.

ISSUES

The issues on appeal are as follows:

Whether claims 1-6, 12-24, and 30 are unpatentable as being obvious over *Noorbakhsh* (US Patent No. 5,699,498) in view of *Rao* (US Patent No. 5,473,566).

GROUPING OF CLAIMS

The claims on appeal stand or fall as a single group.

ARGUMENT

The Office Action rejects claims 1-6, 12-24, and 30 under 35 U.S.C. § 103 as being unpatentable over *Noorbakhsh* (US Patent No. 5,699,498) in view of *Rao* (US Patent No. 5,473,566). This rejection is respectfully traversed.

With respect to all pending claims, the Office Action sates:

> Noorbakhsh teaches a method in a data processing system (computer system, col. 1, lines 13-14) for performing a raster operation (col. 1, line 30) of graphics data, wherein the data processing system includes a system memory (col. 1, line 31-32) and a video memory (36-37), wherein the system memory and the video memory are connected by a bus (system bus, col. 1, line 34, it is noted that

the video memory is not directly connected to the system bus) and wherein the graphics data is organized into picture elements (array of pixels, col. 1, line 41), comprising selecting a first plurality of picture elements from the system memory and selecting a second plurality of picture elements from the video memory (it is noted that Noorbakhsh fails to explicitly suggest or teach "selecting a first and second plurality of pixels from the system and video memories". Noorbakhsh suggests or teaches "reading data from source (system memory) and destination (video) memory areas" (col. 1, lines 25-27). In order to read data from the memory areas, Noorbakhsh must first selected the data and then read the selected data.), wherein "the first and second plurality of picture elements are selected such that changes in a direction of data on the bus are minimized when performing raster operations on the first and second plurality of picture elements." It is noted that in accordance with the present specification, page 12, lines 20-30, this is done by transferring a block of pixels (such as, a scan line) instead of one pixel at time. Noorbakhsh clearly suggests or teaches "bit boundary block transfer (BitBLT) engines are useful in VGA controller (graphics engine) for accelerating BitBLT operations. A BitBLT operation involves a block transfer such as, moving a **rectangle of data** (such as, a scan line) from one area to another" (col. 1, lines 19-24)); reading the first and second plurality of picture elements from the system and video memories (col. 1, lines 25-27). However, Noorbakhsh fails to explicitly suggest or teach **performing a raster operation on a picture element** from the first and second plurality of picture elements to form a processed picture element (col. 1, lines 27-30); and writing the processed picture element to the video memory (col. 1, lines 30-31); and repeating the performing and writing steps for each picture element in the first and second plurality of picture elements until all picture elements have been processed. These are what Rao teaches. Rao teaches these are conventional bit block transfer techniques, where data is moved on a word-by-word or byte-by-byte basis instead of moving data an entire row of data at a time. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Rao into the system of Noorbakhsh because this is a conventional bit block transfer technique as taught by Rao and is considered well known and well use in the art at the time of invention. Rao further teaches an improve Bit block transfer technique by data movement of an entire row if data at a time (col. 7, lines 4 and 8-14). Therefore, at least claims 1-6, 12-24 and 30 would have been obvious by Noorbakhsh and Rao.

Office Action, dated April 30, 2003. Appellant respectfully disagrees. *Noorbakhsh* teaches a technique and apparatus for color expansion into a non-aligned 24-bit RGB (red-green-blue) color space format. *Noorbakhsh* generally teaches about a bit boundary block transfer (BitBLT) technique, which includes transferring rectangular blocks of data from a source memory area to a destination memory area. With respect to BitBLT, *Noorbakhsh* states:

> Bit boundary block transfer ("BitBLT") engines are useful in VGA controllers for accelerating BitBLT operations. In general terms, a BitBLT operation involves a block data transfer such as, for example, moving a rectangle of data from one area of a display memory to another area of the display memory. More particularly, a BitBLT operation comprises a sequence of steps including reading data from a source memory area and data from a destination memory area, logically combining the data respectively read from the source memory area and the destination memory area using one of a number of logical operations generally referred to as raster operations ("ROPs"), and writing the result of the logical operation into the destination memory area.

Noorbakhsh, col. 1, lines 18-30. Thus, *Noorbakhsh* teaches performing both reads and writes as block transfer operations, as part of the BitBLT technique. In other words, raster operations are performed on blocks of picture elements, rather than on a single picture element (pel).

In contradistinction, the present invention provides a method for performing raster operations on graphics data on a pel-by-pel bases, while still performing reads as block transfers. Claim 1 recites:

> 1. A method in a data processing system for performing a raster operation of graphics data, wherein the data processing system includes a system memory and a video memory, wherein the system memory and the video memory are connected by a bus and wherein the graphics data is organized into picture elements, the method comprising the data processing system implemented steps of:
>
> selecting a first plurality of picture elements from the system memory;
>
> selecting a second plurality of picture elements from the video memory, wherein the first plurality of picture elements and the second plurality of picture elements are selected such that changes in a direction of data on the bus are minimized when performing raster operations on the first plurality of picture elements and the second plurality of picture elements;
>
> reading the first plurality of picture elements from the system memory;
>
> reading the second plurality of picture elements from the video memory;
>
> performing a raster operation on a picture element from the first plurality of picture elements and a picture element from the second plurality of picture elements to form a processed picture element;
>
> writing the processed picture element to the video memory; and
>
> repeating the performing and writing steps for each picture element in the first plurality of picture elements and the second plurality of picture elements until all picture elements have been processed, wherein changes in the direction of data on the bus are minimized between the reading and writing of picture elements.

Noorbakhsh does not teach or suggest "performing a raster operation on **a picture element** from the first plurality of picture elements and **a picture element** from the second plurality of picture elements to form **a processed picture element,**" "writing the single processed picture element to the video memory," and "repeating the performing and writing steps for **each picture element** in the first plurality of picture elements and the second plurality of picture elements until all picture elements have been processed," as recited in claim 1. *Noorbakhsh* only teaches performing raster operations as part of bit block transfers. *Noorbakhsh* does not teach or suggest performing raster operations and writes to video memory on a pel-by-pel basis.

Rao teaches a memory architecture including a plurality of shift registers for transferring a row of data, or a plurality of rows, at a time in a bit block transfer, rather than one byte at a time. With respect to BitBLT, *Rao* states:

> Bit block transfer (BitBLT) is an important performance enhancement technique used in digital data processing, graphics and video applications, and in particular in "windowing" applications. In general, in a bit block transfer ("block move"), an entire block of data (also known as bitmaps) is transferred from a first (source) block of storage locations in display memory to a second (destination) block of storage locations in display memory. In graphics systems BitBLTs can improve operational speed since the data transfers typically remain local to graphics controller thereby reducing the tasks required to be performed by the CPU. Similarly, entire blocks of data may be copied from a set of source locations in memory to a set of destination locations in memory by a block copy.

Rao, col. 1, lines 12-25. *Rao* also states:

> The speed of presently available bit block transferring systems is limited by the fact that such systems move or copy data from one address space to another address space in memory on a byte or word basis. Thus, the need has arisen for improved circuits, systems and methods for implementing bit block transfers. In particular, such methods, systems and circuits should be applicable to the movement and/or copying of pixel data within the frame buffer of a display system.

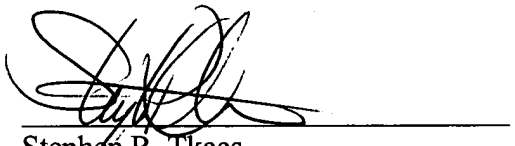
Rao, col. 2, lines 8-16. Thus, *Rao* teaches a memory architecture for more efficiently performing bit block transfers. However, *Rao* does not make up for the deficiencies of *Noorbakhsh*.

The applied references, taken alone or in combination, fail to teach or suggest

"performing a raster operation on **a picture element** from the first plurality of picture elements and **a picture element** from the second plurality of picture elements to form **a processed picture element,**" "writing the single processed picture element to the video memory," and "repeating the performing and writing steps for **each picture element** in the first plurality of picture elements and the second plurality of picture elements until all picture elements have been processed," as recited in claim 1. Both *Noorbakhsh* and *Rao* are directed to conventional BitBLT techniques and, thus, fail to teach or suggest performing raster operations and writes to video memory on a pel-by-pel basis. The applied references fail to teach or suggest each and every claim limitation; therefore, claim 1 is not rendered obvious by the proposed combination of *Noorbakhsh* and *Rao*.

Independent claims 12, 19, and 30 recite subject matter addressed above with respect to claim 1 and are allowable for at least the same reasons. Since claims 2-6, 13-18, and 20-24 depend from claims 1, 12, and 19, the same distinctions between *Noorbakhsh* and *Rao* and the invention recited in claims 1, 12, and 19 apply for these claims.

In view of the above, Appellant respectfully submits that the rejection of claims 1-6, 12-24, and 30 is overcome. Accordingly, it is respectfully urged that the rejection of claims 1-6, 12-24, and 30 not be sustained.



Stephen R. Tkacs
Reg. No. 46,430
Carstens, Yee & Cahoon, LLP
PO Box 802334
Dallas, TX 75380
(972) 367-2001
PO Box 802334
Dallas, TX 75380
(972) 367-2001

APPENDIX OF CLAIMS

The text of the claims involved in the appeal reads:

1. A method in a data processing system for performing a raster operation of graphics data, wherein the data processing system includes a system memory and a video memory, wherein the system memory and the video memory are connected by a bus and wherein the graphics data is organized into picture elements, the method comprising the data processing system implemented steps of:

selecting a first plurality of picture elements from the system memory;

selecting a second plurality of picture elements from the video memory, wherein the first plurality of picture elements and the second plurality of picture elements are selected such that changes in a direction of data on the bus are minimized when performing raster operations on the first plurality of picture elements and the second plurality of picture elements;

reading the first plurality of picture elements from the system memory;

reading the second plurality of picture elements from the video memory;

performing a raster operation on a picture element from the first plurality of picture elements and a picture element from the second plurality of picture elements to form a processed picture element;

writing the processed picture element to the video memory; and

repeating the performing and writing steps for each picture element in the first plurality of picture elements and the second plurality of picture elements until all picture elements have been processed, wherein changes in the direction of data on the bus are minimized between the reading and writing of picture elements.

2. The method of claim 1, wherein the plurality of processed picture elements form a scan line.

3. The method of claim 1, wherein the raster operation performs a logic OR function using a picture element from the system memory and a picture element from the video memory.

4. The method of claim 1, wherein the first plurality of picture elements are part of a source bitmap.

5. The method of claim 1, wherein the second plurality of picture elements are part of a destination bitmap.

6. The method of claim 1, wherein the reading steps, the performing step, and the writing step are performed in a graphics engine.

12. A data processing system comprising:

a bus;

a system memory connected the bus, wherein a first plurality of graphics elements are located within the system memory;

a video memory connected to the bus, wherein a second plurality of graphics elements are located within the video memory;

a processor unit connected to the bus, wherein the processor unit executes instructions to select a first plurality of picture elements from the system memory; select a

second plurality of picture elements from the video memory in which the first plurality of picture elements and the second plurality of picture elements are selected such that changes in a direction of data on the bus are minimized when performing raster operations on the first plurality of picture elements and the second plurality of picture elements; read the first plurality of picture elements from the system memory; read the second plurality of picture elements from the video memory; perform a raster operation on a picture element from the first plurality of picture elements and a picture element from the second plurality of picture elements to form a processed picture element; write the processed picture element to the video memory; and repeat performing and writing for each picture element in the first plurality of picture elements and the second plurality of picture elements until all picture elements have been processed, in which changes in the direction of data on the bus are minimized between the reading and writing of picture elements.

13. The data processing system of claim 12, wherein the first plurality of graphics elements is a plurality of picture elements.

14. The data processing system of claim 12, wherein the first plurality of graphics elements form a scan line.

15. The data processing system of claim 12, wherein the scan line is a scan line in a bitmap.

16. The data processing system of claim 13, wherein the first plurality of picture elements form a bitmap.

17. The data processing system of claim 12, wherein a graphics engine performs the raster operation.

18. The data processing system of claim 12, wherein a video driver performs the raster operation.

19. A data processing system for performing a raster operation of graphics data, wherein the data processing system includes a system memory and a video memory, wherein the system memory and the video memory are connected by a bus and wherein the graphics data is organized into picture elements, the data processing system comprising:

first selecting means for selecting a first plurality of picture elements from the system memory;

second selecting means for selecting a second plurality of picture elements from the video memory, wherein the first plurality of picture elements and the second plurality of picture elements are selected such that changes in a direction of data on the bus are minimized when performing raster operations on the first plurality of picture elements and the second plurality of picture elements;

reading means for reading the first plurality of picture elements from the system memory;

reading means for reading the second plurality of picture elements from the video memory;

performing means for performing a raster operation on a picture element in the first plurality of picture elements and a picture element in the second plurality of picture elements to form a processed picture element;

writing means for writing the plurality of processed picture elements to the video memory; and

repeating initiate of the performing means and writing means for each picture element in the first plurality of picture elements and the second plurality of picture element until all picture elements have been processed, wherein changes in the direction of data on the bus are minimized between the reading and writing of picture elements.

20. The data processing system of claim 19, wherein the plurality of processed picture elements form a scan line.

21. The data processing system of claim 19, wherein the raster operation performs a logic OR function using a picture element from the system memory and a picture element from the video memory.

22. The data processing system of claim 19, wherein the first plurality of picture elements are part of a source bitmap.

23. The data processing system of claim 19, wherein the second plurality of picture elements are part of a destination bitmap.

24. The data processing system of claim 19, wherein the first reading means, the second reading means, the performing means, and the writing means are located in a graphics engine in the data processing system.

30. A computer program product in a computer readable medium for performing a raster operation of graphics data, wherein the data processing system includes a system memory and a video memory, wherein the system memory and the video memory are connected by a bus and wherein the graphics data is organized into picture elements, the computer program product comprising:

first instructions for selecting a first plurality of picture elements from the system memory;

second instructions for selecting a second plurality of picture elements from the video memory, wherein the first plurality of picture elements and the second plurality of picture elements are selected such that changes in a direction of data on the bus are minimized when performing raster operations on the first plurality of picture elements and the second plurality of picture elements;

third instructions for reading the first of a first plurality of picture elements from the system memory;

fourth instructions for reading the second plurality of picture elements from the video memory;

fifth instructions for performing a raster operation on a picture element in the first plurality of picture elements and a picture element in the second plurality of picture elements to form a processed picture element;

sixth instructions for writing the processed picture element to the video memory; and

seventh instructions for initiating the fifth instructions and sixth instructions for each picture element in the first plurality of picture elements and the second plurality of picture elements until all picture elements have been processed, wherein changes in the direction of data on the bus are minimized between the reading and writing of picture elements.